SOLID STATE TRIGGER FOR HIGH POWER THYRATRONS

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ABSTRACT

A simple solid state circuit for pulsing high-power thyratrons is developed. A circuit not optimized for minimum delay and jitter had the following performance: total delay between the input to the pulser and the output of the thyratron is 2 microseconds. The jitter of the thyratron output with respect to the driver input is less than 12 nanoseconds. The circuit has the advantages of low power consumption and long life.

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We recently have been interested in the synchronized pulsing of high power hydrogen thyratrons to drive xenon flash tubes. We had on hand a low level pulse generator (Tektronix 162), and needed a simple way to convert its output to thyratron triggering levels ranging from 400 to 1000 volts at 3 to 10 amperes. Circuits for this purpose are available (Glasoe, 1965), most of which involve using tubes. Tubes have disadvantages: both hard and soft tubes require a filament supply and bias supplies for the various grids, resulting in extra costs (over solid state circuits) in dissipated power, bulk, and components. Tubes also have rather strict limitations on the peak current which can be passed repeatedly, and they have a limited life. Soft tubes which work well with low-level pulses (e.g. 2D21) suffer from an inability to hold off the high voltages needed to trigger high-power thyratrons. Soft tubes which will hold off the required voltage have reduced sensitivity, and generally require an additional driving stage. Hard tubes will hold off the required voltage, but are insensitive and not well suited to pulse service. For these reasons, we turned to a solid state driving circuit.

If peak di/dt is limited, silicon controlled rectifiers (SCR) will pass repeatably and reliably large peak currents; and in conjunction with a transformer to obtain the necessary trigger voltage, SCR's perform admirably as drivers for high-power thyratrons. The need for limiting peak di/dt is discussed by Wechsler (1965), and also in several other papers (Schafft, 1967; Read and Dyer, 1967; Ikeda and Araki, 1967; Somos and Piccone, 1967; Davies and Petruzella, 1967). In the case of SCR's, di/dt failure is caused by hot-spots which develop because the current through the device has become high before the entire gate-cathode junction has been turned on. Overdriving the gate will mitigate the effect (at the expense of gain), but will not overcome it. As a result, it is necessary to analyze the driving circuit to make sure the di/dt through the SCR is kept within reasonable bounds.

The maximum rate of current rise can be determined by solving the network equation for the circuit shown in Figure 1, which is the equivalent circuit for the actual driver shown in Figure 2.

In Figure 1, R and L are the equivalent resistance and inductance seen by the SCR looking into the primary of the pulse transformer. The charging resistor, R_3, is assumed to be large enough to draw little current, and is hence neglected in the analysis. From standard circuit theory,

$$i(t) = \frac{V_o}{L}\left[\frac{1}{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2}\right]^{\frac{1}{2}} \exp\left(-\frac{Rt}{2L}\right) \sin\left[\frac{1}{LC} - \left(\frac{R}{2L}\right)^2\right]^{\frac{1}{2}} t \qquad (1)$$

We can substitute for C in equation (1) the following relation:

$$C = \frac{2E}{V_o^{\,2}} \qquad (2)$$

Where V_o is charging voltage on the capacitor (see Figure 2), and E is the required trigger energy. E can be computed from the relation

$$E = V_t I_t \text{ (pulse repetition rate)} \qquad (3)$$

where V_t is the required trigger voltage and I_t is the required trigger current. Substituting equation (2) into equation (1) and rearranging, we get

$$i(t) = 2\left[\frac{1}{\frac{2L}{E} - \left(\frac{R}{V_o}\right)^2}\right]^{\frac{1}{2}} \exp\left(-\frac{Rt}{2L}\right)\sin\left\{\frac{V_o}{2L}\left[\frac{2L}{E} - \left(\frac{R}{V_o}\right)^2\right]^{\frac{1}{2}}\right\}t \tag{4}$$

As a conservative estimate, assume that the exponential in equation (4) varies slowly enough to be considered constant during the rise time of the pulse. Then from equation (4), the rate-of-change of current through the SCR is:

$$\frac{di}{dt} = \frac{V_o}{L} \cos\left\{\frac{V_o}{2L}\left[\frac{2L}{E} - \left(\frac{R}{V_o}\right)^2\right]^{\frac{1}{2}}\right\}t \tag{5}$$

The maximum value of di/dt, found by setting the cosine term in equation (5) equal to unity, is:

$$\left|di/dt\right|_{max} = V_o/L \tag{6}$$

Manufacturers do not usually specify maximum di/dt values for their SCR's. One exception is the Motorola 2N4199 series of SCR's which are especially designed for high di/dt applications. In this series, the maximum allowable di/dt is 5000 a/microsecond. If we assume that less specialized SCR's will withstand at least one-tenth the di/dt of the 2N4199 series, then from equation (6) we have the relation:

$L_{min} = 2 \times 10^{-9} V_o$, where L_{min} is the minimum circuit inductance allowable for a charging voltage V_o, to protect the SCR from burn-out.

The circuit we have used is shown in Figure 2. The values for the circuit components were chosen under the following constraints: the 5949A requires 5 millijoules of trigger energy. The 2N4195 will hold off 300 volts, thus from equation (2), $C = 0.1$ mfd. The maximum pulse repetition rate is 100 cps, hence $R_3C \leq 0.01$, so $R_3 \leq 10^5$ ohms. The driving transistor should have a low $V_{ce(sat)}$ to make sure the gate-cathode junction is off. A germanium transistor was chosen for this purpose. The value of R_2 was set low enough to insure a large gate drive, to prevent di/dt failure. The trigger transformer can be any convenient unit having sufficient step-up ratio to ensure that the thyratron trigger threshold (600 volts in this case) is exceeded, and also having an inductance greater than $2 \times 10^{-9} V_o$. We used an off-the-shelf photoflash trigger transformer (Anglo MT-55) which easily met both these requirements.

The circuit of Figure 2 has performed quite well for our needs. The delay between the time a drive pulse is applied to the base of the transistor and the time the thyratron reaches maximum current is 2 microseconds, with 200 volts on the SCR. The delay is increased if V_o is reduced, but reliable triggering occurs at voltages as low as 75 volts. The firing delay could be reduced by using a transformer with lower inductance, and an SCR with a faster turn-on time (transistors might also be used). The total jitter of the thyratron output as referenced to the trigger pulse delivered to the base of the transistor was less than 12 nanoseconds. The total power consumption of the driver is less than 5 watts.

In summary, we have developed a simple low-power consumption solid state circuit for driving high power thyratrons. The 2 microsecond delay and 12 nanosecond jitter are acceptible for our purposes, but can be reduced by various techniques (c.f. Charles, 1955), including reduced circuit inductance, a faster switching device, and positive bias on the thyratron.

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I would like to thank Mr. R.T. Kado for his helpful suggestions. This work was supported by Public Health Research Grant No. 1-P07-FR00257 from the Special Resources Branch of the National Institutes of Health and by the National Aeronautics and Space Administration Grant No. NsG 237-62.

FIGURE CAPTIONS

Figure 1. Equivalent circuit for Figure 2.

Figure 2. Drive circuit for high power thyratron.

R_1 = 4.3K	$\frac{1}{2}$W	Q_1 = 2N1306	
R_2 = 270Ω	4W	Q_2 = 2N4195	
R_3 = 50K	1W	V = 5949A (25Kv, 500a max pulse)	
C = 0.1 mfd, 300v		T = Anglo MT-55	
		n = 60, primary impedance = 1 mhy in series with 0.2Ω.	

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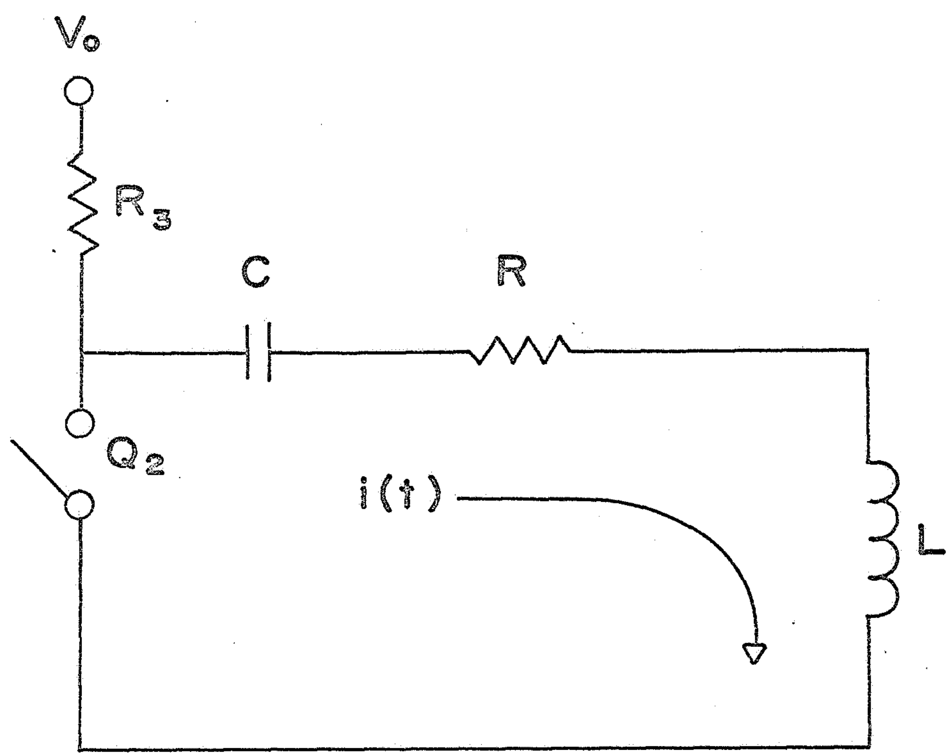
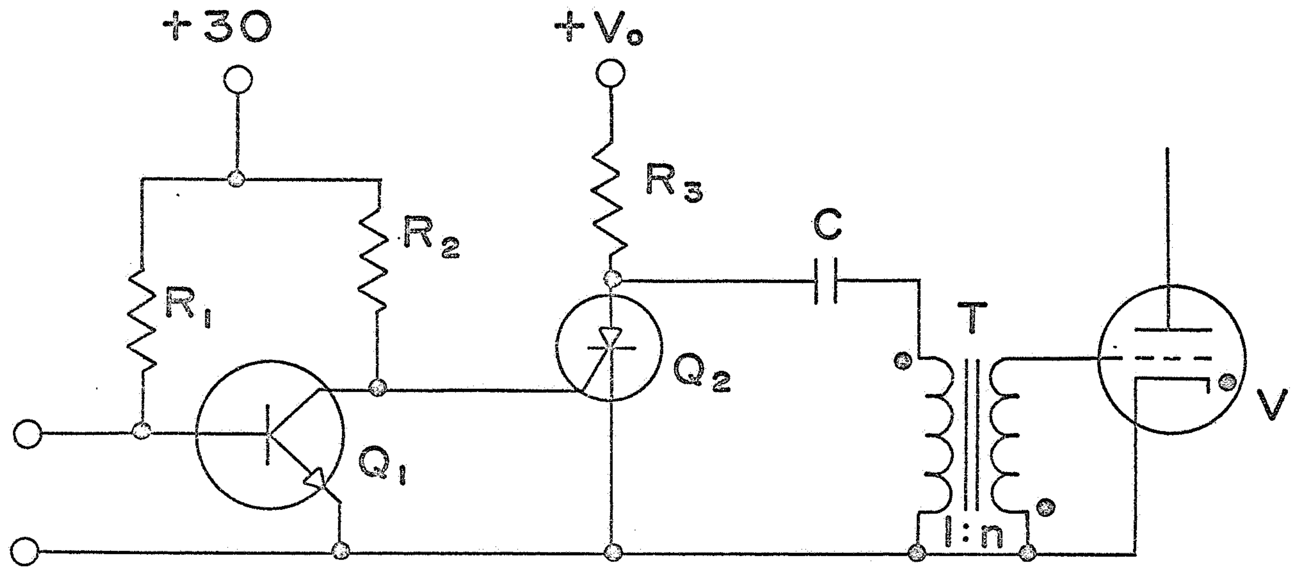


V_0
R_3
C
R
Q_2
i(t)
L



+30
+V₀
R₁
R₂
R₃
C
T
Q₁
Q₂
1:n
V